Development of A Linear Power Amplifier for High Frame Rate Imaging System

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***Abstract* — A linear power amplifier was developed for a high frame rate imaging system. Due to a relatively large number of channels (128) and a high peak power capability of the imaging system (about 300W/channel), the power amplifier was designed to minimize the static power consumption without significant signal distortions. To realize such an amplifier, active bias voltage control of output MOSFETs and output offset adjustment were implemented. A printed circuit board (PCB) was designed and constructed with surface-mount components assembled. The complete amplifier was tested and used with the high frame rate imaging system to obtain RF echo signals for image constructions.**

Keywords-power amplifier; high frame rate imaging system

I. INTRODUCTION

A prototype high frame rate imaging system for imaging of fast moving objects such as the heart has been designed and developed [1]. Although the high frame rate method is capable of construction of three-dimensional (3D) images, as a first step, the high frame rate imaging system was developed for use with 128-element one-dimensional (1D) array transducers for two-dimensional (2D) imaging. To apply the high frame rate imaging method with coded excitation, harmonic imaging, and other medical ultrasound research projects, a linear power amplifier was developed. The specifications of the power amplifier are as follows: (1) wide bandwidth (from 50KHz to over 10MHz); (2) large output voltage at 75 Ohm load with an adjustable power supply voltage up to +/-144V (or a peak power near 300W per channel); and (3) the output changes linearly with a 12-bit D/A converter input without consuming a large static power. Since the number of power amplifiers for the high frame rate imaging system is relatively large and the maximum output voltage is high, a large temperature-dependent static current in the amplifier could result in a high static power that may lead to a hardware failure. For example, with 100mA at +/-144V, each amplifier could consume about 28.8W, and thus 128 amplifiers would require a static power of about 3,686W in total. To avoid this problem, a circuit was designed to automatically control the bias current of the amplifier to a specified low value through an active feedback loop and to minimize the output DC offset voltage to reduce distortions and loss of output dynamic range. The amplifiers have been manufactured and tested. The results are close to the specifications above. In this paper, we will report the design of such an amplifier and its integration with the high frame rate imaging system to produce ultrasound images.

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II. HIGH FRAME RATE IMAGING SYSTEM

A. *High Frame Rate Imaging System*

The high frame rate imaging system consists of broad-band (0.5 – 10MHz), high gain, and 128-channel analog amplifiers, in addition to 128 linear power amplifiers (transmitters). Analog signals from the amplifiers are digitized with 12-bit A/D converters (there are 128 of them) at 40MHz and the digital data of up to 64GB can be stored in the on-board synchronized dynamic random access memory (SDRAM). The range of the analog input signals can be from 30μV to 300mV. The system is controlled by a personal computer (PC) via a standard plug-and-play USB 2.0 link. Videos related to the system design and constructions can be found in Ref. [2].

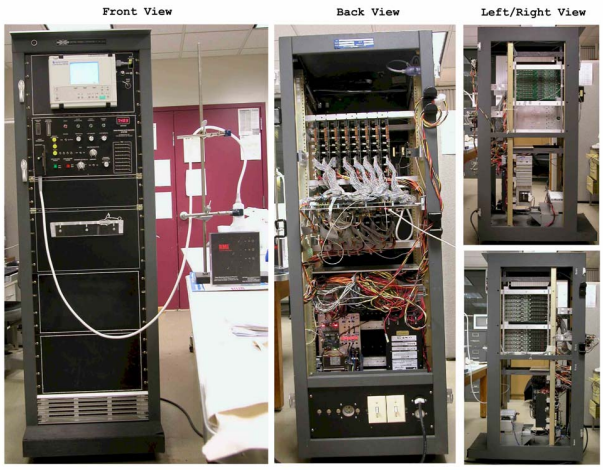


Figure 1. High frame rate imaing system. Front view (left). Back view (middle). Left-side view (top right). And right-side view (bottom right).

B. *Major System Boards*

A number of printed circuit boards (PCBs) have been developed for the high frame rate imaging system. They are: (1) Channel Board – It contains time-variable-gain controlled (TGC) receivers and up to 512MB memory per channel (the TGC amplifiers are controlled via the voltage outputs of 8-bit D/A converters, one for each channel). The boards have 8 routing layers with a high routing and component density. T/R switches are also on this board. (2) Main Board – It is a digital logic control board with 6 routing layers. The board has 8-bit A/D and D/A converters allowing for digitization of electrocardiogram (ECG) signals and the control of voltage of

high-voltage power supplies, respectively. The ECG signals are used to synchronize the high frame rate imaging system with a commercial 12-channel ECG machine for heart imaging. (3) Transmit Board – This is a 6-layer printed circuit board. It is a wideband (0.05MHz to 10MHz), high voltage (up to +/-144V), and linear amplifier, capable of driving 75 Ohm load. The amplifier is driven with a 12-bit/40MHz D/A converter. There is one such amplifier per channel. (4) Front Panel Board – It is a 4-digit LED display constructed on a 4-layer PCB. It also passes signals from the buttons on the front panel to the main board. (5) Power Supply Board – This board is used for an intelligent control of both low-and high-voltage power supplies of the entire imaging system. (6) USB 2.0 Board – It is a 4-layer PCB for communication between the high frame rate imaging system and a PC. This board is also capable of independent use. It contains 12-bit/40MHz A/D and D/A converters with a memory depth of 64 MB and can be controlled by a PC via the USB 2.0 bus.

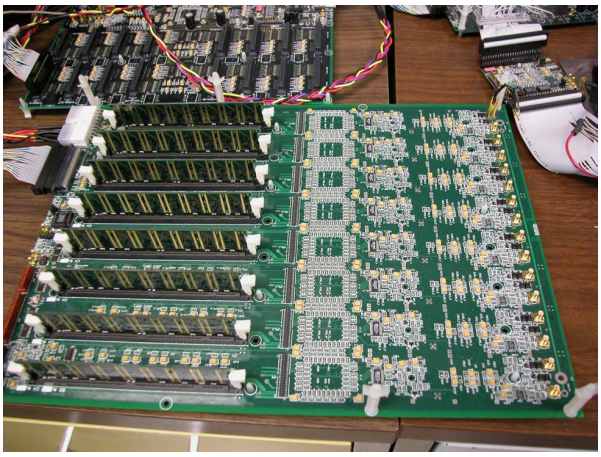


Figure 2. Channel Board. Each channel board contains 8 channels with 8 SDRAM modules (up to 512MB per each module) and 8 active T/R switches. It has 8-layers. The dimension of the board is 15 inch x 11 inch. Each board can also serve as 8 general-purpose ultrasound pulser/receiver with buffered analog outputs, programmable transmission waveforms, and flexible triggering, independent of the main board in Fig. 3.

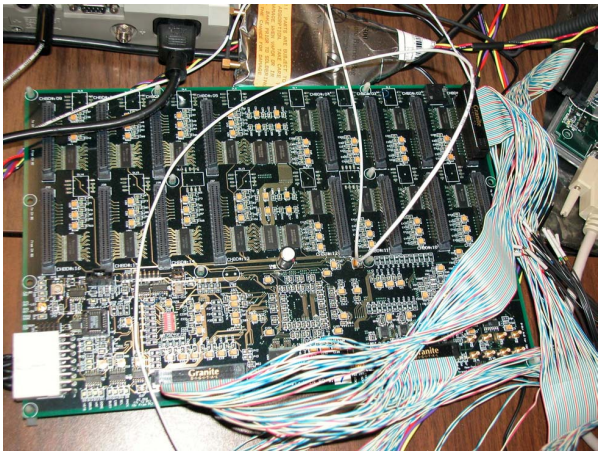
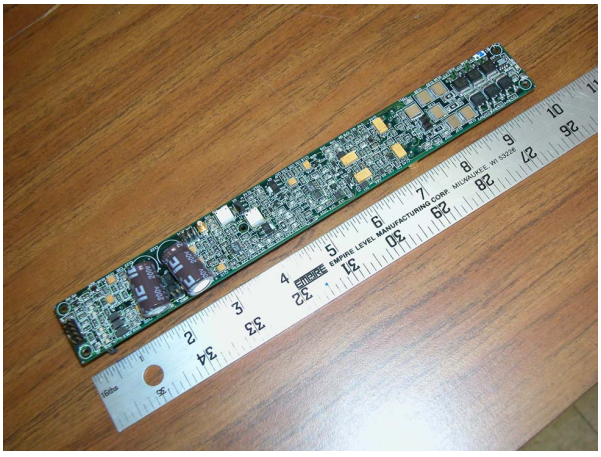


Figure 3. Main board. This board is for the central digital control of the entire imaging system. It is a 6-layer board with a dimension of 12 inch x 8 inch. It contains both 8-bit A/D and D/A converters for digitization of ECG T and TGC signals and for adjustment of voltages of system power supplies. he board could be cascated with one another to support an imaging system of much more than 128 channels in total.



Fi o gure 4. Front view of the linear power amplifier. The amplifier was built n a 6-layer PCB. A 12-bit 40MHz D/A converter is also on the board for generation of arbitrary transmission waveforms for each channel.

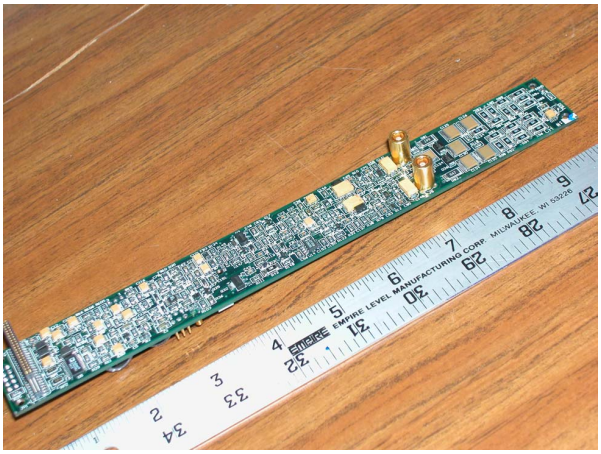


Figure 5. Back view of the linear power amplifier.

Figure 6. Front panel board. The board has a 4-digit LED display for system messages. It contains 8 TGC sliders and passes the signals from the buttons on the fromt panel to the main board.

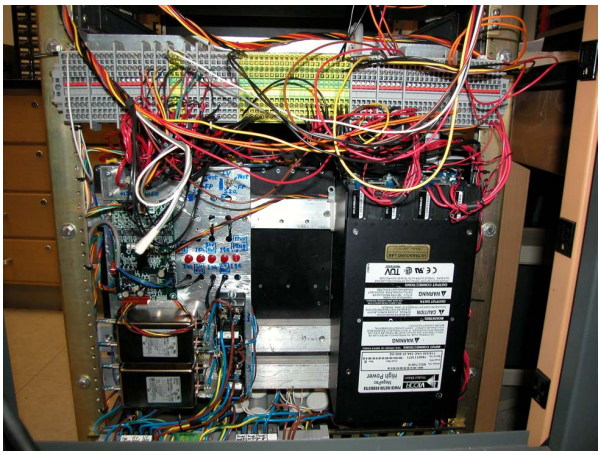


Figure 7. Power supply board. This board serves as an intellegent controller for both low-and high-voltage power supplies of the entire imaging system. (The board is on central left portion of the figure. Surrounding the board are power relays, AC filters, power supplies, and power distribution strips.)

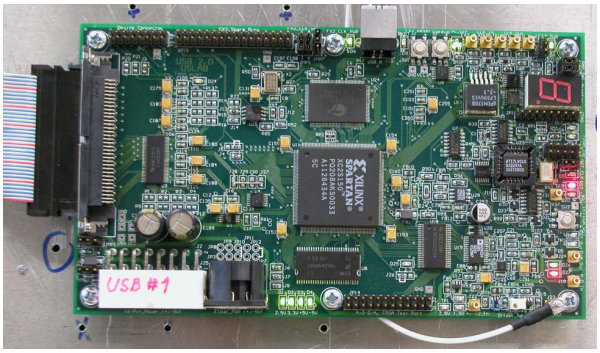


Figure 8. USB 2.0 board. The board is a bridge between a PC and the high frame rate imaging system. It also can be used independently. It has a 40MHz A/D and D/A with 64MB of memory depth and can be controlled by a PC via the USB 2.0 bus for data acquisition and a linear control.

This work was supported in part by a grant, HL60301, from the National Institute of Health of USA.

III. Design of Power Amplifier

As mentioned in the introduction, it is desirable to have low static power consumption while maintaining a low distortion for the power amplifiers since the number of channels in the system is relatively large. A large static power may overheat the imaging system and thus lead to a hardware failure. In addition, the thermal runaway of the static working point may increase the static power after an increase of temperature. Therefore, to have an active control for low static power and to avoid thermal runaway of the power amplifiers are important. The active bias control of the power amplifier was realized using a current feedback loop and a switching circuit that can distinguish between bias current and the low-frequency transmission signals. An active output offset control loop was also designed to have enough loop gain to reduce the loss of output dynamic range while maintaining system stability (avoid oscillations).

IV. Data Acquisition And Image Construction

The power amplifiers were mounted on top of each channel board to complete the high frame rate imaging system. The imaging system was used to obtain digitized RF echo data at a high frame rate (a few thousand frames per second depending on the depth of the image and the field of view) for image construction.

Figure 9. Experiment setup for data acquisition using the high frame rate imaging system. A standard RMI tissue mimicking phanton was used in the experiment. RF data were acquired with a 3.5MHz and 128-element broadband array trnasducer.

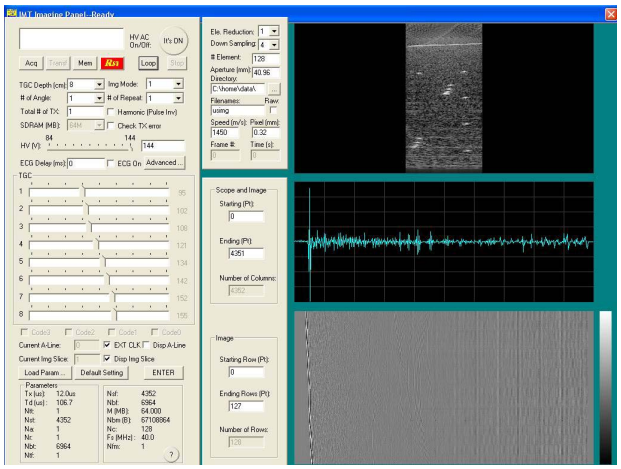


Figure 10. Constructed image with RF echo data shown on a PC running Microsoft Windows Xp. The PC program serves as a graphic user interface between users and the high frame rate imaging system. The control panel is shown on the left hand side of the figure. The TGC control can be applied from the control panel as well as from the front panel of the machine. An image constructed with the high frame rate imaging method [1] is at the top-right of the figure. In the middle-right, a RF echo signal from one of the transducer elements is shown. The bottom-right panel shows RF echo signals from all of the channels (each horizontal line represents an echo from a transducer element and the relationship between echoes can be clearly seen).

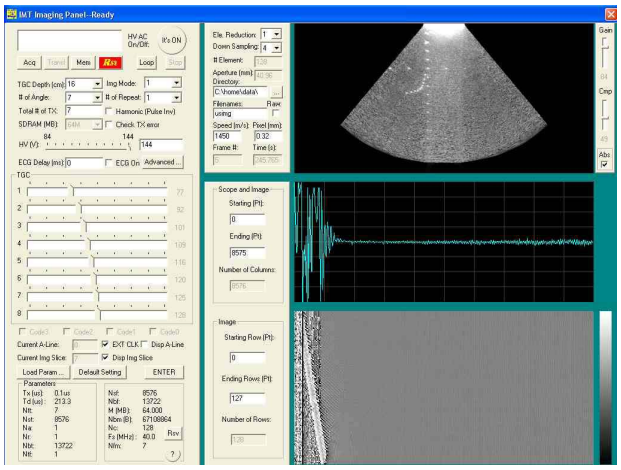


Figure 11. Images constructed from multiple transmission angles with the high frame rate imaging method [1]. Plane waves (no transmission focusing) were used in transmissions.

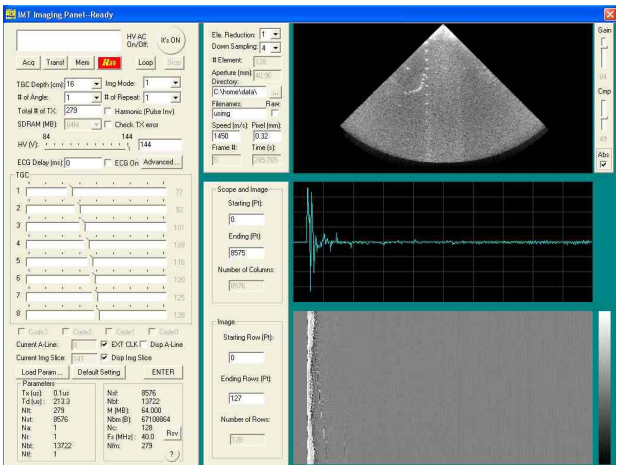


Figure 12. Images constructed with the conventional delay-and-sum (dynamic focusing) method in reception with a tranmission focus at about 5cm from the apix of the imag (the depth of the image shown is about 16cm).

V. CONCLUSION

The power amplifiers developed meet the design specifications and were successfully tested along with the entire imaging system.

ACKNOWLEDGMENT

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REFERENCES

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